

LAYER DESCRIPTION	COPPER +PLATING WT	SE IMP OHMS	SE TRACE WIDTH	DIFF IMP OHMS	DIFF TRACE WIDTH/SPACE	REF LAYER
L01 - TOP	1.850 Mils	--	-----	USB-90ohm	6 mils/6.5 mils	L02 - GND1
L02 - GND1	1.260 Mils	--	-----	---	----	--
L03 - SIG_PWR	1.260 Mils	--	-----	USB-90ohm	6 mils/6.5 mils	L02 - GND1
L04 - PWR	1.260 Mils	--	-----	---	----	--
L05 - GND2	1.260 Mils	--	-----	---	----	--
L06 - BOTTOM	1.850 Mils	--	-----	---	.-----/.-----	--

STACK-UP

NOTES: UNLESS OTHERWISE SPECIFIED

1. SPECIFICATIONS/TOLERANCES:
   A. FABRICATE PER IPC-6012, CLASS 2, USING PROVIDED DATA FILES 610-60658-01.ZIP
   B. ALL SPECIFICATIONS USED SHALL BE PER THEIR LATEST REVISIONS.
   C. THE DIMENSIONS OF CIRCUIT FEATURES IN THE PROVIDED DATA MAY BE ADJUSTED ONLY TO COMPENSATE FOR PROCESS TOLERANCES; ADDING, REMOVING OR RELOCATING CIRCUIT FEATURES, INCLUDING NON-FUNCTIONAL PADS, IS NOT ALLOWED, AND THE DESIGN OF ALL PLANE STRUCTURES MUST BE MAINTAINED TO ENSURE PROPER ELECTRICAL PERFORMANCE.
   D. REMOVE ALL BURRS AND BREAK SHARP EDGES, .381 [.015] MAX RADIUS.
   E. PARENTHETICAL INFORMATION IS FOR REFERENCE ONLY.
   F. REPAIR OF PCB DEFECTS IS NOT PERMITTED.

2 DIELECTRIC MATERIAL:
   A. DIELECTRIC MATERIAL SHALL BE PER IPC-4101/99, /124, /126 OR /129 (RoHS COMPLIANT EPOXY-GLASS).RoHS LOGO SHOULD BE PRINTED ON PCB.
   B. MINIMUM DIELECTRIC THICKNESS SHALL BE .051 [.002] FOR REFERENCED STACK-UP DIMENSIONS OF.076 [.003] OR GREATER; IPC-6012 REQUIREMENTS SHALL OTHERWISE APPLY. SINGLE-PLY CONSTRUCTION IS ALLOWED.
   C. SEE LAYER STACK-UP FOR REQUIRED COPPER WEIGHTS AND THE FINISHED PCB THICKNESS. IF SPECIFIED, 1/3 OZ. STARTING FOIL MAY BE ACHIEVED BY 1/2 OZ. FOIL REDUCTION.
   D. FINISHED PCB THICKNESS SHALL BE MEASURED OVER LANDS AND/OR CONDUCTORS NOT COVERED BY SOLDER MASK.

3. DRILLING:
   A. VIA DIAMETERS (TOL. = +.051/- DRILL DIAMETER [+.0020/- DRILL DIAMETER]) SHALL BE VERIFIED BEFORE PLATING; ALL OTHER HOLE DIAMETERS SHALL BE VERIFIED AT FINAL INSPECTION.
   B. LAYER-TO-LAYER MISREGISTRATION SHALL BE .127 [.005] MAXIMUM.
   C. FILL ALL THRU VIAS USING NON-CONDUCTIVE EPOXY AND OVERPLATE WITH COPPER, .005 [.0002] MINIMUM THICKNESS. DIMPLE DEPTH IN BGA PADS SHALL BE .025 [.001] MAXIMUM. THE PRESENCE OF WRAP PLATING SHALL BE VISUALLY EVIDENT IN ALL QUALITY CONFORMANCE MICROSECTIONS; NO MINIMUM MEASUREMENT REQUIRED.

4. SOLDER MASK:
   A. APPLY LPI SOLDER MASK USING PROVIDED DATA.
   B. SOLDER MASK SHALL BE PER IPC-SM-840, CLASS T, COLOR BLUE.
   C. THE DIMENSIONS OF SOLDER MASK-DEFINED PADS ON PLANES AND/OR WIDE CONDUCTORS SHALL NOT BE MODIFIED.

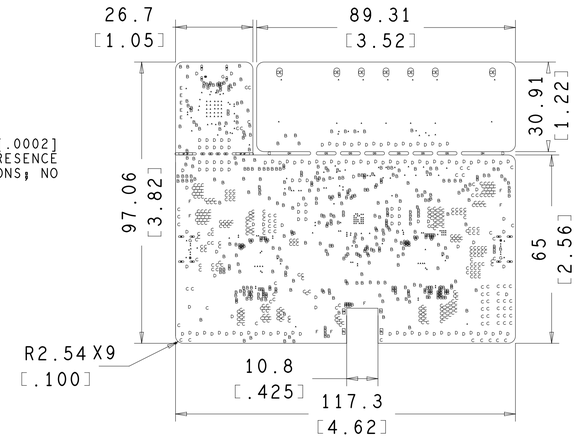
5. MARKING:
   A. MARK PCB PER PROVIDED DATA USING SILKSCREEN OR AUTOMATED INJET PROCESSING WITH PERMANENT, NON-CONDUCTIVE INK, COLOR WHITE.
   B. SUPPLIER ID AND TRACEABILITY INFORMATION SHALL BE APPLIED USING PERMANENT, NON-CONDUCTIVE INK, COLOR WHITE.
   C. INK SHALL NOT BE APPLIED TO ANY SOLDERABLE SURFACE.

6. ELECTRICAL TEST:
   A. DESIGN VERIFICATION SHALL BE DONE PRIOR TO PCB FABRICATION USING SUPPLIED VALOR ODB++ DATABASE, OR GERBER DATA AND AN IPC-D-356 NETLIST.
   B. ALL PCBS SHALL BE 100% ELECTRICALLY TESTED FOR OPENS AND SHORTS USING PROVIDED DATA.
   C. APPLY TEST STAMP IN NON-LEGEND AREA ON REAR SIDE OF PCB; OK TO APPLY TO PANEL RAILS IF SPACE DOES NOT PERMIT.

7 FINAL FINISH:
   A. FINAL FINISH SHALL BE ELECTROLESS NICKEL/IMMERSION GOLD (ENIG) PER IPC-4552.

8. IMPEDANCE:
   A. IMPEDANCE TOLERANCE SHALL BE +/- 10%.
   B. SEE LAYER STACK-UP FOR IMPEDANCE REQUIREMENTS.

9. IF PANELIZATION SPECIFICATIONS ARE PROVIDED, THE PCBS SHALL BE DELIVERED IN PANEL FORM. HOWEVER, THESE SPECIFICATIONS MAY BE CHANGED AS REQUIRED BY THE CONTRACT MANUFACTURER TO SUPPORT VOLUME ASSEMBLY REQUIREMENTS.



DRILL CHART: TOP to BOTTOM				
ALL UNITS ARE IN MILS				
FIGURE	FINISHED_SIZE	TOLERANCE_DRILL	PLATED	QTY
A	8.0	+3.0/-3.0	PLATED	223
B	10.0	+3.0/-3.0	PLATED	464
C	15.0	+3.0/-3.0	PLATED	387
D	40.0	+3.0/-3.0	PLATED	146
E	43.307	+3.0/-3.0	PLATED	5
F	51.201	+3.0/-3.0	PLATED	7
G	23.618	+2.0/-2.0	NON-PLATED	3
H	55.118x39.37	+3.0/-3.0	PLATED	1
J	62.988x23.618	+3.0/-3.0	PLATED	2
K	62.988x23.618	+3.0/-3.0	PLATED	4
L	70.866x39.37	+3.0/-3.0	PLATED	1
M	74.799x23.618	+3.0/-3.0	PLATED	2
N	74.799x23.618	+3.0/-3.0	PLATED	4
P	78.74x39.37	+3.0/-3.0	PLATED	2
R	33.461x23.618	+2.0/-2.0	NON-PLATED	2
S	33.461x23.618	+2.0/-2.0	NON-PLATED	1
T	60.0x30.0	+2.0/-2.0	NON-PLATED	4
U	120.0x80.0	+2.0/-2.0	NON-PLATED	7
V	240.0x30.0	+2.0/-2.0	NON-PLATED	4
W	270.0x45.0	+2.0/-2.0	NON-PLATED	6
X	580.0x45.0	+2.0/-2.0	NON-PLATED	2

TOTAL HOLES: 1277

SEE BOM	SEE BOM
NEXT ASSY	USED ON
APPLICATION	

THE INFORMATION CONTAINED HEREIN IS CONFIDENTIAL AND PROPRIETARY TO CYPRESS SEMICONDUCTOR AND SHALL NOT BE REPRODUCED OR DISCLOSED IN WHOLE OR IN PART OR USED FOR ANY DESIGN, MANUFACTURE, OR OTHERWISE, EXCEPT WHEN SUCH USER POSSESSES AUTHORIZATION FROM CYPRESS

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN METRIC WITH INCHES IN BRACKETS
.XXX ±.064 [±.005] .XX ±.13 [±.01] ANGLES ±.5°

MATERIAL 2

FINISH 7

DO NOT SCALE DRAWING

APPROVALS	DATE
DRAWN HUSA	06/06/24
ENGINEER HUSA	06/06/24
APPROVED GUBILI	06/06/24
QA -	-
PROJ. ENG. -	-

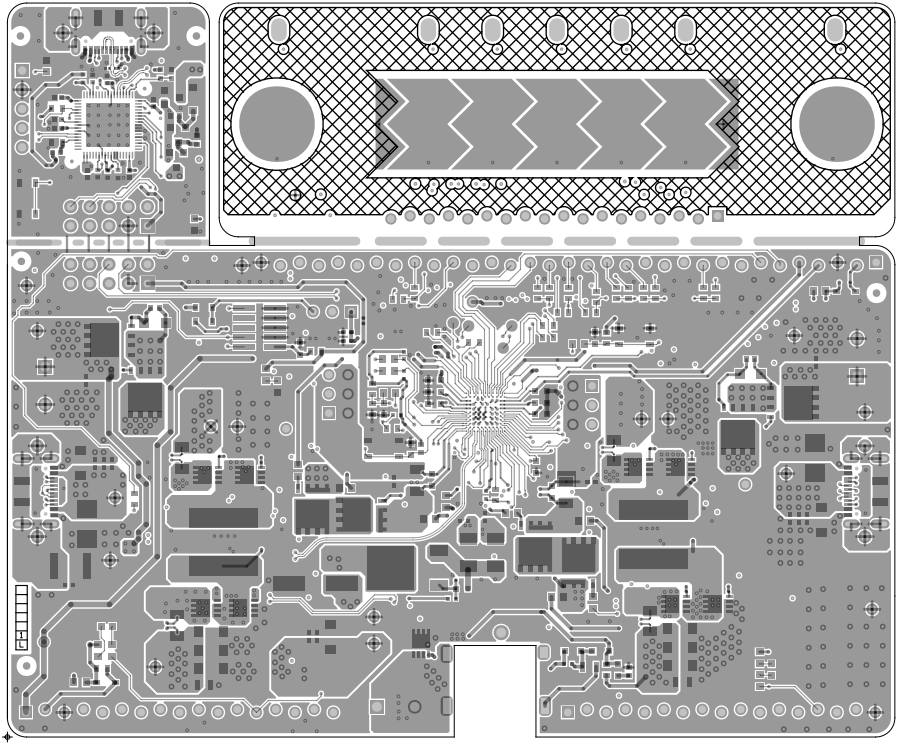
198 CHAMPION COURT
SAN JOSE, CA 95134
(408) 943-2600

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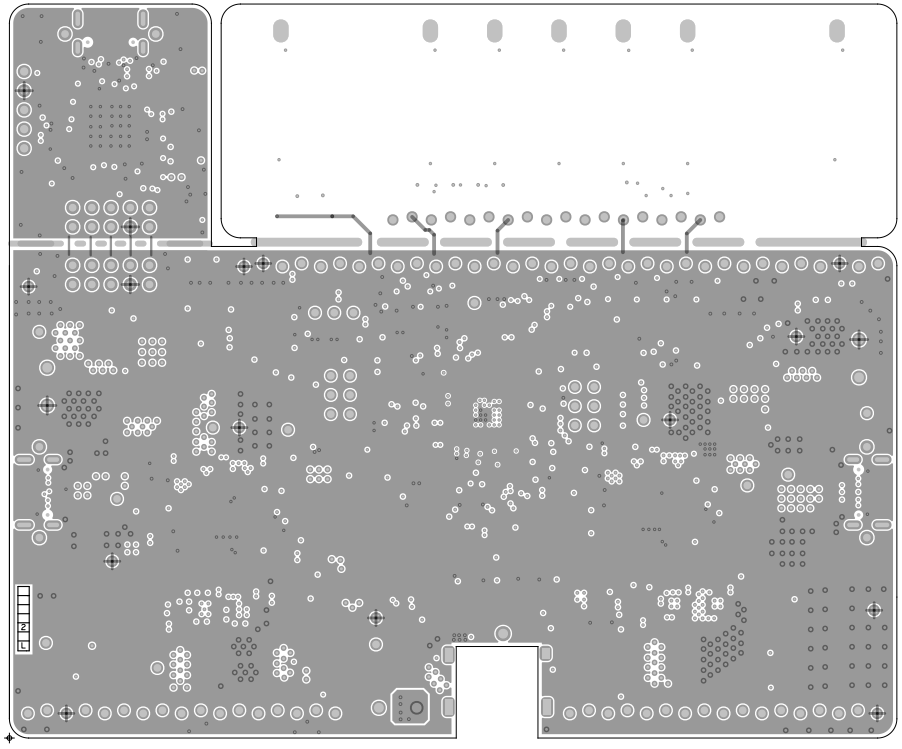
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SCALE	SHEET	REV
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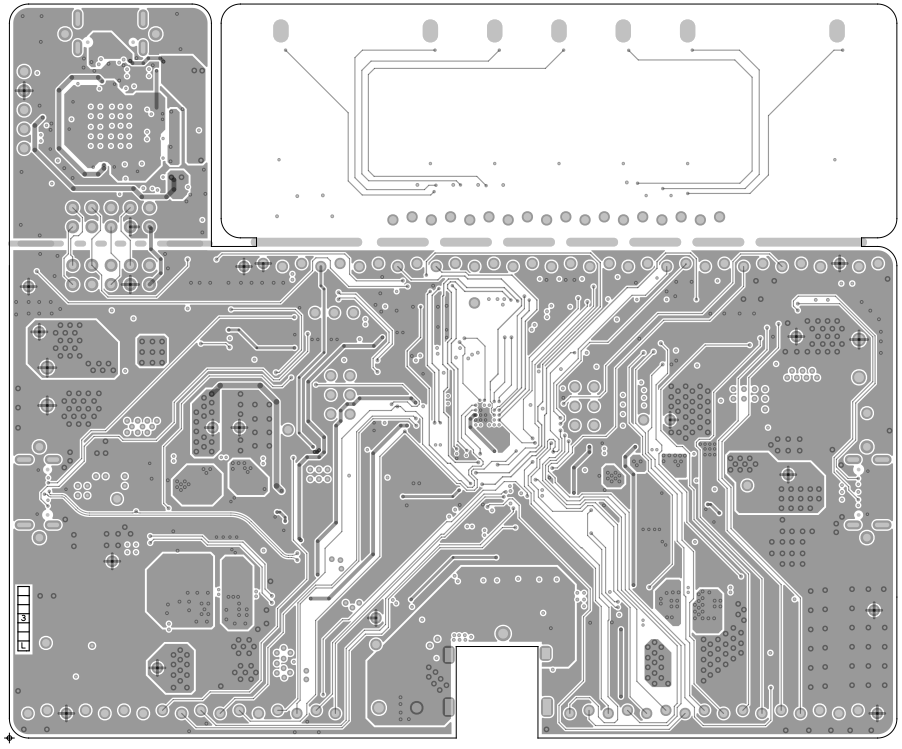
COMPUTER GENERATED DRAWING
DO NOT CHANGE MANUALLY



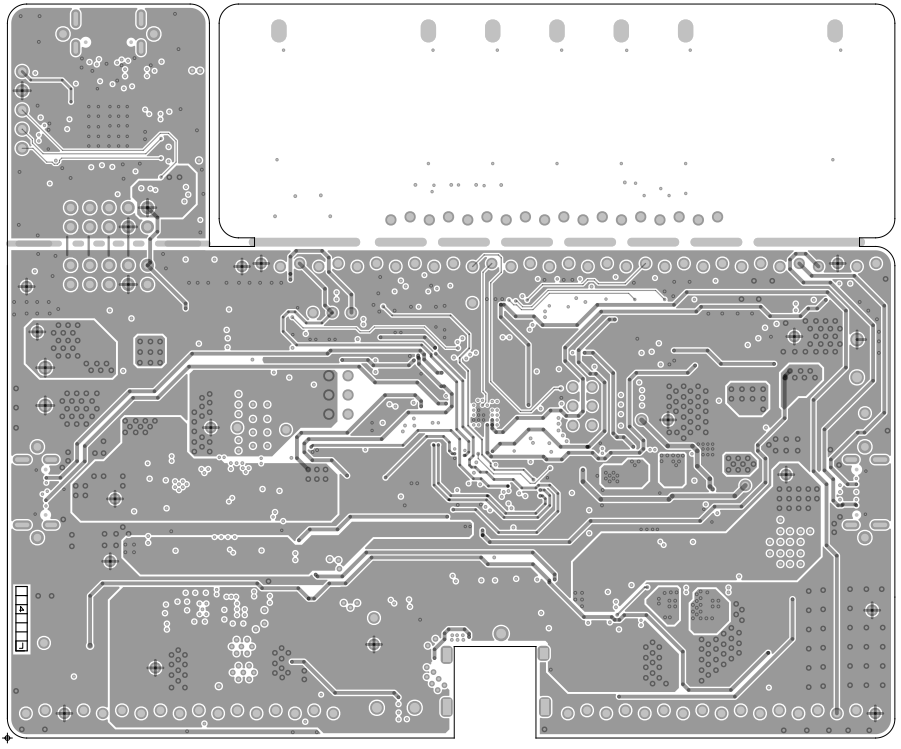
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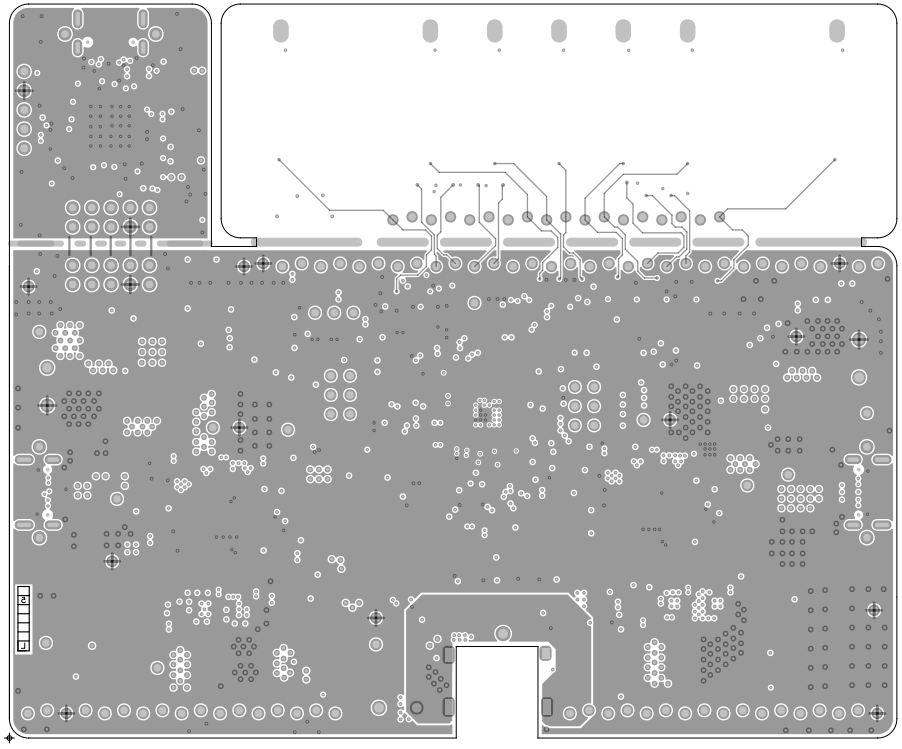
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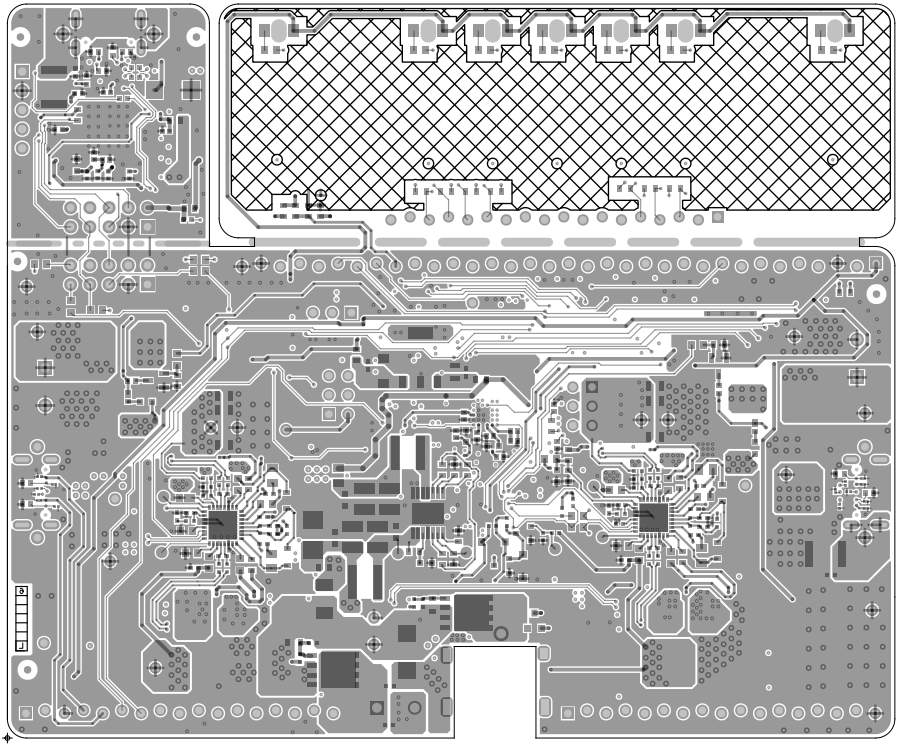
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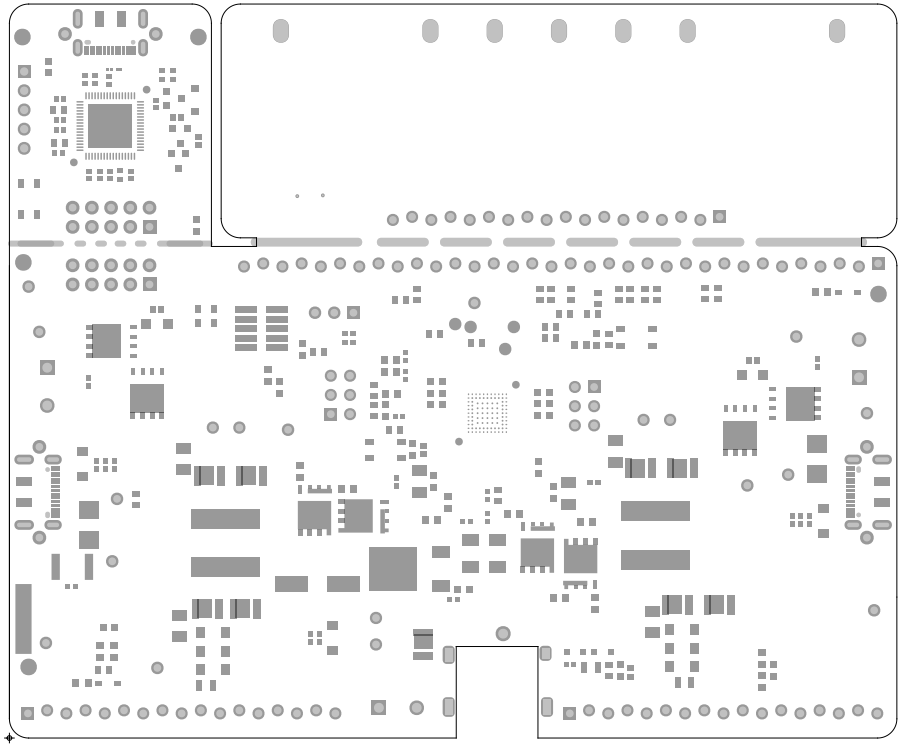
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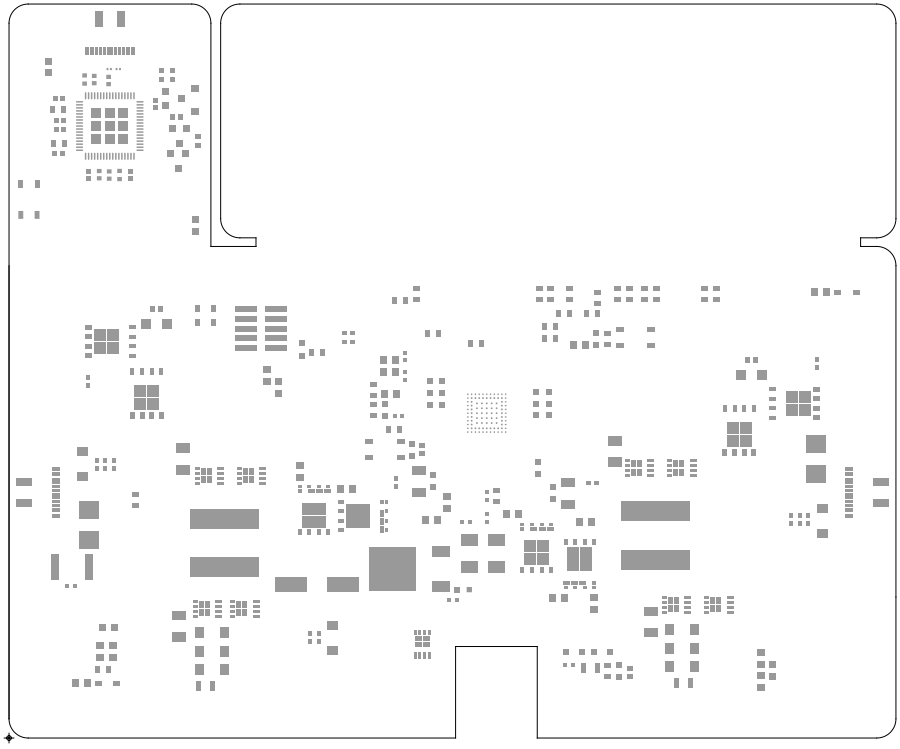
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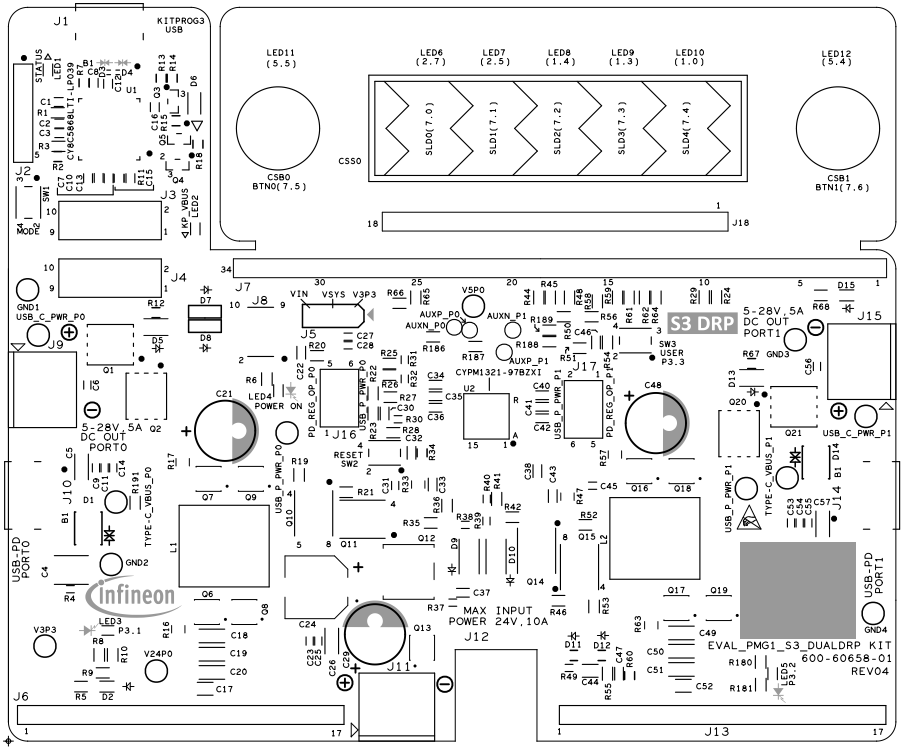
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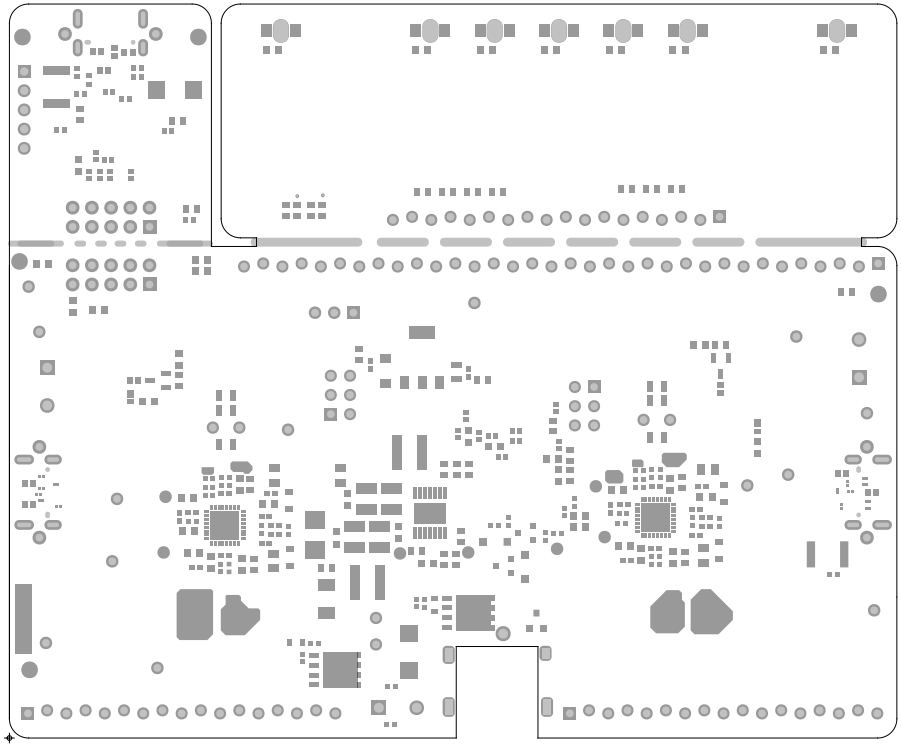
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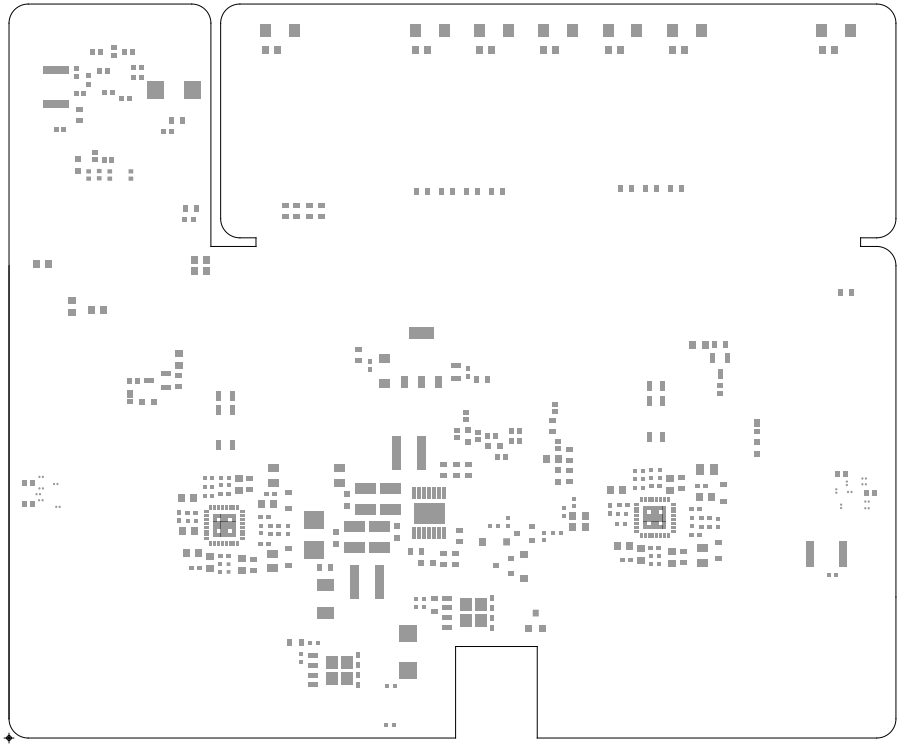
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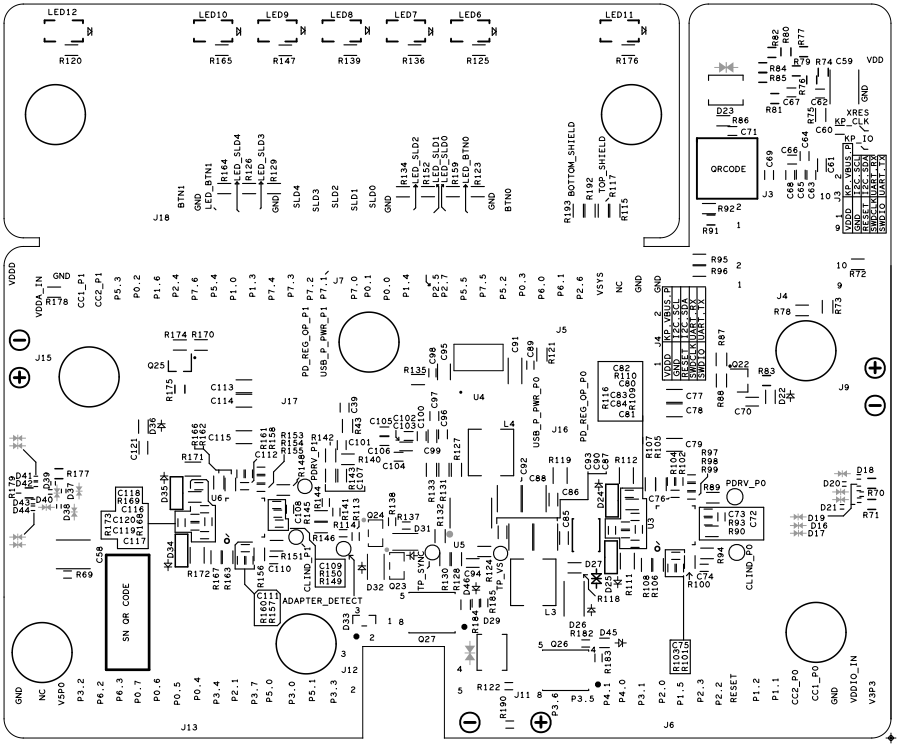
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SAN JOSE, CA 95134 (408) 943-2600	DWG NO: 600-60658-01	REV:04	DATE:06/06/24



SAN JOSE, CA 95134 (408) 943-2600	PROJECT:EVAL_PMG1_S3_DUALDRP KIT		
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	LAYER:MOTTOM BOTTOM SOLDERMASK		
	DWG NO: 600-60658-01	REV: 04	DATE:06/06/24



SAN JOSE, CA 95134 (408) 943-2600	PROJECT:EVAL_PMG1_S3_DUALDRP KIT		
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Infineon SAN JOSE, CA 95134 (408) 943-2600	DWG NO: 600-60628-01	REV:04	DATE:06\06\24
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